

ELECTRONICS LAB MANUAL

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Fifth Edition

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Book Descriptions:

Digital Electronic Lab Manual Pdf

NAME OF EXPERIMENT PAGE NO. NO. Introduction to DIGITAL ELECTRONICS lab nomenclature of DIGITAL ICS, 1 specifications, study of the data sheet, concept of vcc and ground, 36 verification of the truth tables of logic gates using TTL ICS. The NOT OR operation is known as NOR operation. Logic Symbol of Gates LAB manual IV SEM ECE Page3. PRECAUTIONS 1. Make the connections according to the IC pin diagram. 2. The connections should be tight. 6 3. The Vcc and ground should be applied carefully at the specified pin only. DIGITAL ELECTRONICS LAB Quiz Questions with answer. Define gates Ans. Gates are the DIGITAL circuits, which perform a specific type of logical operation. Define IC Ans. IC means integrated circuit. It is the integration of no. DIGITAL ELECTRONICS LAB EXPERIMENT NO 2 Aim Implementation of the Given Boolean Function using Logic Gates in Both Sop and Pos Forms. APPARATUS REQUIRED Power Supply, DIGITAL Trainer, IC s 7404, 7408, 7432 Connecting leads. BRIEF THEORY Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an nvariable Kmap there are 2 cells. Each cell corresponds to one of the combination of n variable, since there are 2 combinations of nvariables. 8 Gray code has been used for the identification of cells. PRECAUTIONS 1 Make the connections according to the IC pin diagram. 9 2 The connections should be tight. 3 The Vcc and ground should be applied carefully at the specified pin only. Quiz Questions with answer. Define Kmap Ans. It is a method of simplifying Boolean Functions in a systematic mathematical way. Define SOP Ans. Sum of Product. Define POS Ans. Product of Sum. What are combinational circuits Ans. These are those circuits whose output depends upon the inputs present at that instant of time. What are sequential circuits Ans. <http://www.zscamke.sk/userfiles/bunn-cdbcf15-manual.xml>

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These are those circuits whose output depends upon the input present at that time as well as the previous output. If there are four variables how many cells the Kmap will have Ans. 16. When two minterms can be adjacent Ans. 2 to the power n. Which code is used for the identification of cells 10 Ans. 8. Gray Code. Define Byte Ans. Byte is a combination of 8 bits. The knobs on the right side of the box allow manual adjustment Power Electronics Laboratory Manual. Safety is always important when working with electricity and electronics.. Welcome to the ECE 111 lab manual ! Most of the projects in this lab manual. Experiments in Digital Fundamentals, a laboratory manual by David. Figure 10 depicts the function generator in lab. Figure 10 HP33120A Function Generator. Discover everything Scribd has to offer, including books and audiobooks from major publishers. Start Free Trial Cancel anytime. Report this Document Download Now Save Save Digital electronics lab manual.pdf For Later 100% 1 100% found this document useful 1 vote 247 views 94 pages Digital electronics lab manual.pdf Uploaded by Ramkumar Sivakaminathan Description Digital electronics lab manual Full description Save Save Digital electronics lab manual.pdf For Later 100% 100% found this document useful, Mark this document as useful 0% 0% found this document not useful, Mark this document as not useful Embed Share Print Download Now Jump to Page You are on page 1 of 94 Search inside document Browse Books Site Directory Site Language English Change Language English Change Language. <http://www.nam.org.np/userfiles/bunn-cds-2-parts-manual.xml>

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 binaryAlso exercise loading only one of multiple values into theRealize theAlso to construct and 8to1
 multiplexer and 1 to 8Construct a 4bit binaryAlso exercise loading only one of multiple values into the
 The breadboard consists of two terminal strips and two bus strips oftenEach bus strip has two
 rows of contacts.

Each of theThat is, each contact along a row on a busBus strips are usedEach terminal strip has 60
 rowsEach row of 5You will build your circuits on the terminal strips by inserting the leads ofFig 1.
 The breadboard. The lines indicate connected holes.ICs Integrated circuits used during the
 experiments. Incorrect connection ofBuilding the Circuit. Throughout these experiments we will use
 TTL chips to build circuits. ThePoint all theTurn the power off immediately before you begin to
 rewire theCommon Causes of ProblemsTo study the working of 5v DC Power supply. Tools Required
 Connecting Wires, Multimeter, Stepdown transformer,Circuit Diagram. Stepdown Transformer. It is
 used to step down the voltage of A.C. Signal. Here we areIt converts 230v A.C. signal into 9v
 A.C.Bridge Rectifier. It converts A.C. signal into D.C. signal. It is full wave Rectifier. Here it converts
 9v A.C. signal to 9v D.C. signal. Capacitors. After rectification, we dont get the perfect D.C. signal;
 there isIt works as a. Filter.LED turns on when the circuit gets power. Conclusion. We get 5v D.C.
 voltage across the output which can be used as a 5v. D.C. power supply.OBJECT To investigate AND,
 OR, NOT, Exclusive OR EXOR. Exclusive NOR EXNOR, NAND and NOR Gate operationNOT
 gate7404. OR gate7432. NAND gate7400. NOR gate7402. EXOr gate7486. EXNOR gate74266Output
 of ORPin no 7 is grounded and 14 isInput pins are 1,2, 4,5,9,10,12,13 and output of these nandIn
 this IC nor gate input isPin no 7 is grounded and 14 isInput pins are 1,2, 4,5,9,10,12,13 and output
 of these nandIn this IC nor gateUser IC should be tested in test socketEXPERIMENT No.2. OBJECT
 To verify the truth table of AND, OR, NOT, ExOR, ExNOR realized using. NAND and NOR gatesNOR
 gate7402. NOT gate7404Output of NAND gate will be 1 if anyone of the. NAND gate then output is
 given asOutput of NOR gate will be 1 only when all inputs areImplementing Inverter using NAND
 Gate.

<https://www.informaquiz.it/petrgenesis1604790/status/flotaganis20052022-0140>

The figure shows two ways in which a NAND Gate can be used as an inverterImplementing AND
 Gate using NAND Gate. An AND Gate can be realized by NAND Gate with its output complemented
 byAn OR Gate can be realized by NAND Gate with all its inputs complementedThe figure shows two
 ways in which a NOR Gate can be used as an inverterImplementing OR Gate using NOR Gate. An OR
 Gate is realized by NOR Gate with its output complemented by a NOR. Gate inverter. Implementing

AND Gate using NOR Gate. An AND Gate is realized by NOR Gate with all its inputs complemented by a NOR Gate inverter. Implementing ExNOR Gate using NOR Gate. Precautions Result The basic logic gates are successfully constructed using NAND Boolean function without using any other gate. Since NAND and NOR are AND gate 7408. XOR gate 7486 etc. A half adder adds two one-bit binary numbers A and B. It Fig. 1.1 Half adder logic diagram. From the truth table, the logic expression for the Sum output can be written as a Sum of Product expression by summing up the input combinations for which the sum is equal to 1. Now, this expression can be simplified as. Similarly, the logic expression for Carry output can be expressed as a Sum of Product Fig. 1.2 Full Adder logic diagram. From the truth table, the logic expression for S can be written by summing up the input A B S Sum C Carry A B C in S Sum Cout Carry NOT gate 7404 etc. One full adder is responsible for the addition of two binary. The carryout of one stage is fed directly to the carryin. It is composed of four full. The carry out is then transmitted to. The final result creates a sum of four bits plus a carry. Pin Diagram Also to construct. The function of. Multiplexer is to select one of the input lines and connect it to the output.

<http://www.compass-it.com/images/Delonghi-Ro2058-Manual.pdf>

It is also known. The select input is controlled by. The select input code determines to which. In other words, demultiplexer takes one input. The number of select. Data input Select inputs Outputs OBJECT Study of Binary to Gray and gray to binary code converter and also verify the truth. The gray code is OR gates i.e. one ExOR gate IC. Viva Quiz THEORY 1 RS FlipFlop To synthesize a D. It has only one. It is very useful when a single data bit 0 or 1 is to be stored. If there is a HIGH on the D input when a clock pulse is applied, the flipflop SETs and stores. If there is a LOW on the D input when a clock pulse is applied, the flipflop RESETs and. The truth table below summarize the operations of the positive edge triggered D flipflop. The Flip flop has been used in. How it is removed. Count sequence for a binary ripple counter. A2 will go from 1 to 0 and complement A3. A2 will go from 1 to 0 and complement A3. A3 will go from 1 to 0 and complement A4. Every time A2 goes from 1 to 0, it A1 is complemented with the count. As a result A2 goes. A3 now goes from 1 to 0, which complements. A4. The output transition of A4, if connected to a next stage, will not trigger the next flip. The count of a 4-bit. A list of the count sequence of a count down binary counter shows that the lowest order bit. Any other bit in the sequence is. Then when Q goes from 0 to 1, Q will. THEORY The Shift Register. The Shift Register is another type of sequential logic circuit that is used for the storage or. The Shift Register is used for data storage or data movement and are used in calculators or. Serial in to Parallel out SIPO. The operation is as follows. Let's assume that all the flipflops FF A to FF D have just been. Assume now that the DATA input pin of. The effect of each clock pulse is to shift the data contents of each stage one place to the right. Clock Pulse No QA QB QC QD If yes, explain how. Now customize the name of a clipboard to store your clips. I have Thousands of hard covers may not be included.

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questions given at the end of each experiment will be very helpful for the students. Apparatus Required Procedure IC 7483, IC 7404, etc. 1. Apply the inputs to A0 to A3 and B0 to B3. 2. Connect C0 to the Ground. 3. Check the output sum on the S0 to S3 and also C4. 4. For subtraction connect C0 to Vcc, Apply the B input through NOT gate, which gives the complement of B. 5. The truth table of adder and Subtractor are noted down. Truth Table for Subtractor A3 A2 A1 A0 B3 B2 B1 B0 C4 S3 S2 S1 S 15 Conclusion . To study and verify the truth table of excess3 to BCD code converter Apparatus Required IC 7400, IC 7404, etc. Apparatus Required IC 74153, IC 74139, IC 7404, etc. Making Ea and Eb zero and the output is taken at Za, and Zb. 8. In full adder using MUX, the input is applied at Cn1, An and Bn. APPARATUS REQUIRED IC 7400, IC 7410, IC 7420, etc. PROCEDURE 1. Connections are made as shown in the Circuit diagram. 2. Change the values of the inputs as per the truth table and note down the outputs readings using multimeter. Apparatus Required IC 7486, IC 7404, IC 7408, etc. APPARATUS REQUIRED IC 74148, IC 7447, 7segment display, etc. PROCEDURE Encoder 1. Connections are made as per circuit diagram. 2. The octal inputs are given at the corresponding pins. 3. The outputs are verified at the corresponding output pins. PROCEDURE Decoder 1. Connections are made as per the circuit diagram. 2. Connect the pins of IC 7447 to the respective pins of the LED display board. 3. Give different combinations of the inputs and observe the decimal numbers displayed on the board. RESULT The given octal numbers are converted into binary numbers. Procedure 1.

Connections are made as per circuit diagram. 2. The truth table is verified for various combinations of inputs. Apparatus Required IC 7408, IC 7476, IC 7490, IC 74192, IC 74193, IC 7400, IC 7416, IC 7432 etc. Apparatus Required IC 7495, etc. Serial In Serial Out 1. Connections are made as per circuit diagram. 2. Load the shift register with 4 bits of data one by one serially. 3. At the end of 4 th clock pulse the first data d0 appears at QD. 4. Apply another clock pulse; the second data d1 appears at QD. 5. Apply another clock pulse; the third data appears at QD. 6. Application of next clock pulse will enable the 4 th data d3 to appear at QD. Left Shift 1. Connections are made as per circuit diagram. 2. Apply the first data at D and apply one clock pulse. This data appears at QD. 3. Now the second data is made available at D and one clock pulse applied. The data appears at QD to QC and the new data appears at QD. 4. Step 3 is repeated until all the 4 bits are entered one by one. 5. At the end 4 th clock pulse the 4 bits are available at QA, QB, QC and QD. Apparatus Required IC 7495, IC 7404, etc. Apparatus Required IC 7495, IC 7486, etc. Procedure 1. Connections are made as per the circuit diagram. 2. Clock pulses are applied one by one and truth table is verified. Apparatus Required IC 555 timer, resistor, capacitor, etc. Apparatus Required IC 2114, etc. Procedure 1. circuits connections are made to the appropriate pins of IC First you have to write the data and then read the data, for writing data make WE to low and CS input to low 3. for a 4bit data select any address input from A0 to A9. Conclusion. Signature of the staff in charge Asynchronous Counters Become familiar with the most common digital components and their use. Equipment 1 st. LED bridge 1 st. 7segment display. 2 st. IC Chapter 10 Counters.

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counter count This document supplements it. When you write add DD R0, R1, R2, you imagine something like this R1 Like registers, the state, or the flipflop values themselves, serves as the output. The output value increases by one on each clock cycle. The number of flipflops used and the way in which they are connected determine the number of states and also ECE124 Digital Circuits and Systems Page 1 S Active high set and reset signals. S ECE124 igital Circuits Dr. I. J. Wassell Electronic Engineering A Module SE42205 Digital Design Cubic dice similar to modern dice date back to before It stores program data and the results.

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